Design and Analysis of Conventional P-FF using 90 nm CMOS Technology

Sonam Parihar
P.G student, Bipin Tripathi Kumaon Institute of Technology, Dwarahat, Almora, Uttarakhand, India.

Rachana Arya
. Assistant Professor, ECE Deptt, Bipin Tripathi Kumaon Institute of Technology, Dwarahat, Almora, Uttarakhand, India.

Abstract – Over the last four decades the integrated circuit industry has evolved in a tremendous pace. This success has been driven by the scaling of device sizes leading to higher and higher integration capability, which have enabled more functionality and higher performance. The impressive evolution of modern high performance microprocessors have resulted in chips with over a billion transistors as well as multi-GHz clock frequencies. Different logic has emerged as a major area of research due to its ability to reduce the power dissipation which is the main requirement in the low power digital circuit design. It has wide applications like low power CMOS design, Nano-technology, Digital signal processing. In this paper, I will design (modify) and analysis the Conditional Discharging Flip flop circuit, at the simulation TSMC 90nm technology for 1.8 V.

Index Terms – Flip flop, Conditional discharge, power consumption, Pulse triggered.

1. INTRODUCTION

Low power industry is growing at a very rapid rate. One of the factors behind this rapid growth is the hand held devices which operate on battery. The battery technology has not improved as compared to VLSI also if we employ more power to batteries there is a risk of explosion, so we have the only option i.e. to design new low power circuits and design techniques. With an increasing demand for higher performance and lower power dissipation in current microprocessor, new circuit design techniques are needed for both switching logic and storage devices. In a digital system, flip-flops are often thought of as memory devices, whose primary function is to store state information and data results. *As* complexity in microprocessor increases, both logic requirements and storage depth Swill also increase. This will lead to a larger number of flip-flops and may result in larger power consumption. In fact, the maximum speed of a flip-flop is directly proportional to the total power dissipated. In the mobile part used in today's computer notebooks, emphasis on power dissipation has been a major primarily design concern.

In the past, the major concerns of the VLSI designer were area, performance, cost and reliability, power consideration was mostly of only secondary importance. In recent years, however; this has begun to change and, increasingly, power is being given comparable weight to area and speed considerations. Several factors have contributed to this trend. Perhaps the primary driving factor has been the remarkable success and growth of the class of personal computing devices (portable desktops, audio- and video-based multimedia products) and wireless communications systems (personal digital assistants and personal communicators) which demand smaller devices with complex functionality and low power consumption.

Flip flop design are basic storage elements used in all types of digital design. Flip flop design and performance has a effect in reducing the power dissipation and in high performance system. Microprocessors basically uses master slave and pulse triggered flip flop. Master slave are made up of two stages, one master and one slave characterized by their hard-edge property. Pulse triggered reduces two stages into one and are characterized by soft-edge property. Pulse triggered is more popular than master slave because of its single latch structure and high speed operation. The main advantage of pulse triggered is that it allow time borrowing across cycle boundaries which leads to high performance. Pulse triggered flip flop can be static, or semi-static, or dynamic, or semi dynamic. Pulse triggered flip flop can also be classified into single-edge triggered flip flop and double edge triggered flip flop. On the basis of location of pulse generator they are classified as implicit pulse triggered and explicit pulse triggered flip flop. In implicit the pulse is generated inside the flip flop where as in explicit pulse is generated outside the flip flop. Implicit are more economical but suffer from a problem of long discharge. Explicit incurs more power consumption but the logic separation from latch design gives the flip flop design a unique speed advantage.

2. CONVENTIONAL FLIP FLOPS

Here in this section few existing design are discussed for the purpose of comparison.

2.1 Conventional Explicit-Type P-FF Design

Figure 2.1, shows a classic explicit P-FF design, named data-close to- output (ep-DCO). Its latch design is a NAND-logic-based pulse generator and a semi dynamic true-single-phase-clock (TSPC) structured. By sharing a single pulse generator among a group of flip-flops the pulse generator power consumption can be significantly reduced. Ep-DCO shares a single pulse generator among a group of flip flops to improve energy efficiency In this P-FF design, data latching is done with the help of inverters I3 and I4 and inverters I1 and I2 are used to hold the internal node X. The delay of three inverters determines the pulse width. The drawback of this design is that on every rising edge of the clock pulse the internal node X is discharged in spite of the presence of a static input "1". Due to this large switching power is dissipated.

To overcome this problem, many techniques such as conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme have been proposed.

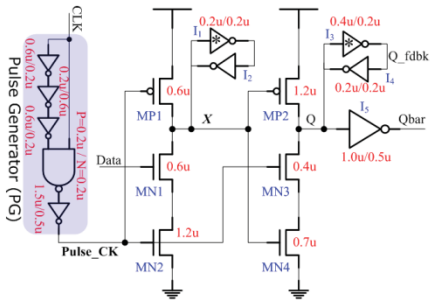

Figure 3.1. ep-DCO

2.2 Conditional Discharge flip flop

To overcome the problem encounter in ep-DCO, and to reduce redundant switching activities techniques were presented, conditional capture, conditional precharge and conditional discharge

A. Conditional capture:

This technique is used for controlling the internal node in the pre charge path in sequential element. The general idea about technique is that the pre-charging path is controlled to avoid precharging the internal node. Referring to Figure 3.2, we can see that the D input is given to the first NMOS in the PDN network. When this input is high , the output should be high too. The clock input to the PMOS will charge the output node to high when clock is low. There is no need to charge the output to high again if D input is already high. Thus, there can be a power reduction in the flop by controlling this behavior. To control the internal node in the precharge path, a control switch is used as shown in Figure 3.2. Only a transition that is going to change the state of the output is allowed. As one of the input to flops is the clock, considering the clock (Clock signal) is the element that makes the most transition in a system, a technique for example conditional pre-charging can significantly help reduce power. The drawback of this technique is that, this is not applicable for implicit flip flop.

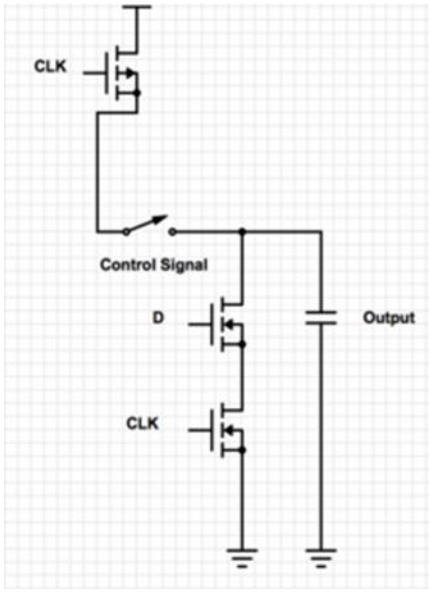

Figure 2.2.Conditional precharge technique

B. Conditional Capture Technique:

This technique is mainly applied for implicit pulse triggered flip flop to prevent any necessary internal node transition. From Figure 3.3, we can see that for controlling the switching of the internal nodes a control signal is applied. The clock is supplied to two NMOS in series.

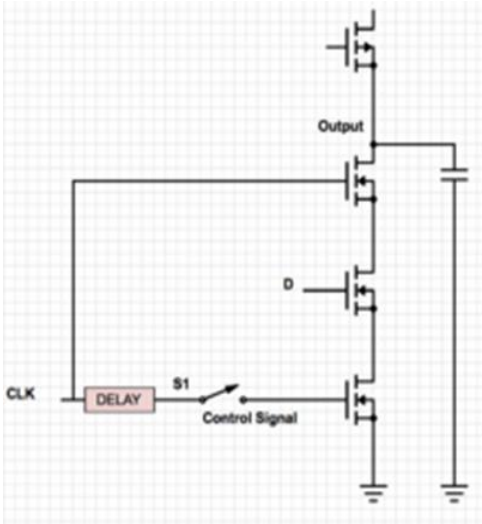

Figure 2.3. Conditional capture technique

The discharge path will not be complete till the control signal allows the last NMOS to be on. This control signal could be generated by a simple circuitry, with its inputs being the present output, input and the state of the clock (high or low). There is no need to cause a state transition when the output of the flop is low, and high clock pulse is applied with the input being a low pulse. The extra computation to sample the inputs cause a increase in setup time of the flop , this is a disadvantage of this technique.

C. Proposed Conditional Discharge technique:

Due to the disadvantage of above two technique conditional discharge technique is proposed for both implicit and explicit pulse triggered flip flop. In this technique, the extra switching activity is eliminated by controlling the discharge path when the input is stable high. Here extra nMOS is inserted in the discharge path.

CDFF uses a pulse generator which is suitable for double edge sampling. Flip flop is made up of two stages. Stage 1 is responsible for capturing the low to high transition whereas stage 2 captures high to low transition. If input is high, internal node X is discharged, as a result, output node will charged to high through MP2 in second stage. If input D is low, first stage disabled, X retain precharge state whereas Y will high and the discharge path in second stage will be enabled allowing the output node to discharge and correctly capture the input data.

If input makes a Low to High transition, the clock pulse is high, MN1 , MN2 and MN3 switch on, the internal node X is discharge to low. For this transition (low to high), X is discharged only once. To ensure that D high to low transition is sampled by the flip flop, dual path is used. By employing the dual path, capacity at node X is reduced and thus the low to high delay could be reduced. Such node X is not charged and discharged every clock cycle, no glitches appear at the output node. Thus, CDFF features less noise generation. CDFF is suitable for both speed critical paths and speed-insensitive paths for energy-efficiency.

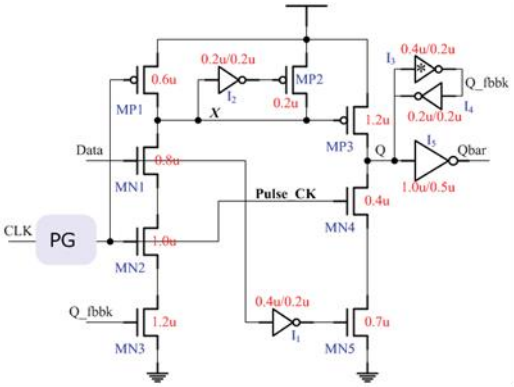

Figure 2.4. CDFF

2. 3. Static conditional discharge flip flop

SCDFF and CDFF are almost similar, the difference is only in their latching structure. Figure 3.5 shows almost similar to CDFF but with changed position of static latch and node X having keeper logic as two back-to back end inverters. Here node X is not periodically precharge and it also exhibit longer D to Q delay. The problem with both designs is the three stacked transistor in the discharging path i.e MN1-MN3.

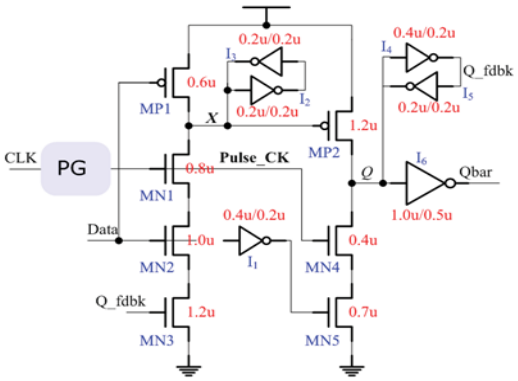

Figure 2.5. SCDFF

3.4. Modified Hybrid Latch Flip Flop

To overcome this delay MHLFF is introduced [10]. MHLFF also uses static latch. The keeper logic at X in SCDFF is removed in MHLFF. When Q is zero a weak pull-up transistor MP1 controlled by the FF output signal Q is used to maintain the node X level at high. This design eliminates the unnecessary discharging problem at node X. The design circuit complexity is high when compare with the other techniques.

However, this design encounters two drawbacks. First, during "0" to "1"transitions a longer Data-to-Q (D-to-Q) delay is expected because node X is not pre-discharged. When a level-degraded clock pulse is applied to discharging MN3 this delay deteriorates further. Larger transistors MN3 and MNZ are required to enhance the discharging capability.

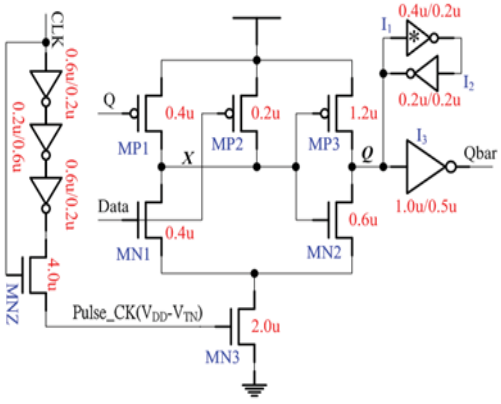

Figure 2.6. MHLFF

Second, when output Q and input Data both equal to "1" node X becomes floating. Because of this its value may drift causing extra Dc power.

3. SIMULATION RESULTS

The simulation results for all the flip flop were obtained in a 90nm CMOS technology at room temperature using Tanner Tool 13, the supply voltage is 1.8V. A clock frequency of 250MHz is used for single-edge triggered flip flops, whereas double-edge triggered flip flops uses a a frequency of 125MHz. Comparison table shows the simulation results of various flip flops. In view of power consumption and PDP, CDFF has least value as compare to other flip flop.

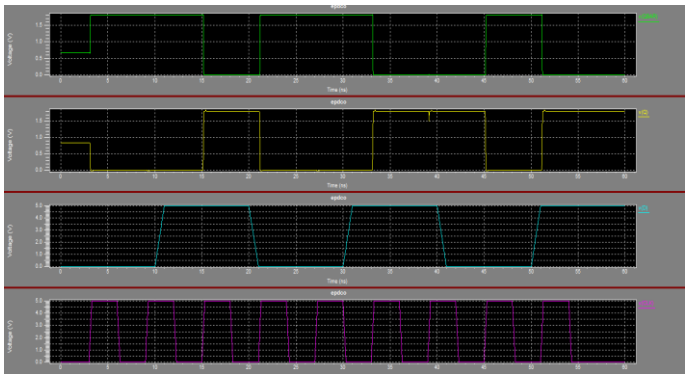

Figure .3.1. Waveform of ep-DCO.

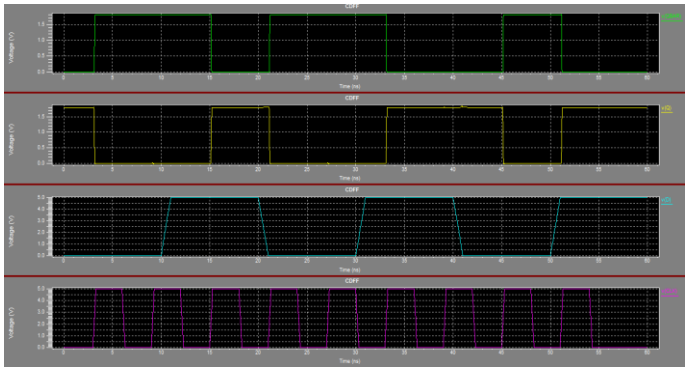

Figure 3.2 Waveform of CDFF.

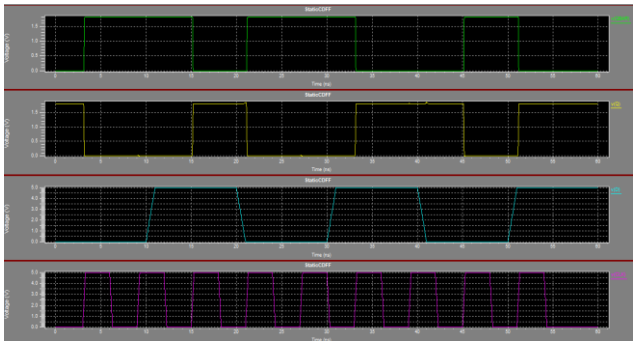

Figure.3.3.Wavefrom of Static-CDFF.

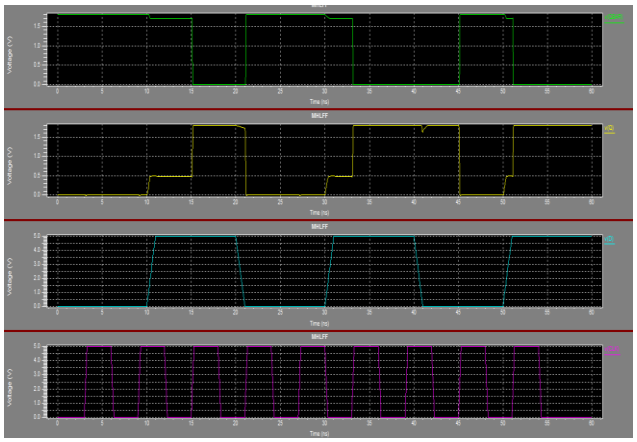

Figure.3.4. Waveform of MHLFF.

4. CONCLUSION

In this paper, four flip flops are studied and compared. Both single edge and dual edge clocked flip flop are discussed. Dual edge triggered clocked flip flop consumed less power. Delay, number of transistor, average power consumed and power delay product of different flip flops designs is compared. The quality and performance of a CMOS process and gate design is measured in terms of power-delay product. The power-delay product can be interpreted as the average energy required for a gate to switch its output from low to high and from high to low. The simulation is performed in 90nm technology CMOS technology, using power supply of 1.8V and clock frequency of 250MHz.

REFERENCES

[1] Jin-Fa Lin, "Low-Power Pulse-Triggered Flip-Flop Design Based on a Signal Feed-Through Scheme" IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 22, No. 1, January 2014.

[2] P. Zhao, T. Darwish, M. Bayoumi ,"High-performance and low power conditional discharge flip-flop", IEEE Trans. Very Large Scale Integration. (VLSI) Syst., Vol. 12, No. 5, pp. 477–484, May 2004.

[3] JuhiRastogi, vipul Bhatnagar,"Low power high performance pulse FF based on signal feed scheme" IJATES, vol 3, issue no 01, March 2015.

[4] Yin-Tsung Hwang, Jin-Fa Lin and Ming-HwaSheu. "Low-power Pulse-triggered flip flop Design with Conditional Pulse-Enhancement Scheme" IEEE Transaction On Very Large Scale Integration (VLSI) Systems, Vol. 20, No. 2, January 2014.

[5] Kanika Jindal,Renu,V K Pandey,"Design of Conditional Data Mapping Flip Flop for Low Power Applications," IJISME,vol 1, issue 5, April 2013.

[6] CMOS Digital Intergrated Circuits, Analysis and Design by Sung-Mo Kang and Yusuf Leblebici.

[7] Nitin Kumar Singh Chauhan , Anshul Jain, "Comparative Analysis of low area and low power D Flip-Flop for Different Logic Values", The International Journal Of Engineering And Science (IJES), Volume . 3, Issue 8,Pages 15-19,2014 .